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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/577,007	05/24/2000	Kazuyoshi Fujioka	829-551	5218

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EXAMINER
SCHECHTER, ANDREW M

ART UNIT	PAPER NUMBER
2871	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/577,007	FUJIOKA ET AL.
	Examiner	Art Unit
	Andrew Schechter	2871

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 August 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-7 and 9-14* is/are allowed.

6)☒ Claim(s) *8 and 15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *11* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 12 August 2002 have been fully considered but they are not persuasive.

Regarding claim 1, the applicant has amended to add the limitation that "the continuous electrode pattern for adsorbing an ionic impurity is provided on only one of the substrates and is at least partially coplanar with the pixel electrodes". Neither *Kikuchi* nor *Tanaka* discloses a continuous electrode pattern surrounding the display pixel area on all sides on only one of the substrate. *Kikuchi* shows the pattern on both substrates along only one edge, while *Tanaka* shows a discontinuous pattern which is on the lower substrate on the right and left sides, while on the upper substrate on the top and bottom sides. Claim 1 is therefore allowable, as are claims 2-7, 11, and 14 which depend on it.

Similarly, the applicant has amended claim 10 to add the limitation that the electrode pattern is "on only one of the substrates, said pattern being coplanar with the pixel electrodes". Since the claim recites the electrode pattern being on only one of the substrates, and both *Kikuchi* and *Tanaka* disclose having it on both substrates, claim 10 is also allowable.

Claim 8 has been amended to add "wherein all segments of the electrode pattern ... are provided on the same substrate and are at least partially coplanar with the pixel electrodes..." The claim does not state that there is not another electrode pattern on

the opposite substrate, so the plurality of segments on the lower substrate in *Tanaka* satisfy the present claim language. *Tanaka* has the electrode pattern [4] coplanar with the address lines, and the applicant argues erroneously that "*Tanaka* teaches directly away from" having them coplanar with the pixel electrodes. This is incorrect: *Tanaka* does not even disclose pixel electrodes; so there can be no teaching in *Tanaka* that having the electrode pattern coplanar with the pixel electrodes is a bad idea. The mere fact that *Tanaka* shows them coplanar with the address lines is not evidence that the inventors of *Tanaka's* device would avoid making them coplanar with the pixel electrodes were they making the combination recited in the previous rejection; the examiner argues below that the opposite is in fact true.

Claim 15 add the limitation that the electrode pattern is "at least partially coplanar with the pixel electrodes". It does not require that the electrode pattern be entirely on one substrate, so it is still unpatentable over *Tanaka* in the same way claim 8 is.

The applicant has amended claims 12 and 13 to clarify that the electrode patterns on either 2 or 3 particular sides of the display are only along those 2 or 3 sides of the display, which is not taught by the prior art (*Tanaka* disclose the electrode pattern on all four sides, *Kikuchi* discloses it only on one side). Therefore, claims 12 and 13 are now allowable.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 8 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Mitsui*, U.S. Patent No. 5,408,345 in view of *Kikuchi et al.,* Japanese Patent Document 5-323336, and *Tanaka*, Japanese Patent Document No. 4-295824.

Mitsui discloses [see Figs. 4-6, for example] a liquid crystal display device comprising a pair of substrates [31, 45], a liquid crystal layer [49], switching elements [40], gate and source lines [32, 39], interlayer film [42] partially covering the address lines, and pixels [38] over the gate/source lines. Further, it discloses that the pixels overlap the gate or signal lines, that the pixel electrodes are reflective, and that the interlayer film is organic. *Mitsui* does not disclose an electrode pattern for adsorbing an ionic impurity on the interlayer insulating film in the surrounding region. Regarding claim 15, *Mitsui* also does not disclose that it surrounds the display area on all sides and is at least partially coplanar with the pixel electrodes. Regarding claim 8, it also does not disclose that the pattern is in segments, the segments being on the same substrate, and partially coplanar with the pixel electrodes on a different elevation that the gate signal lines.

However, it would have been obvious for one of ordinary skill in the art to provide such an electrode pattern, as taught by *Kikuchi* (and *Tanaka*). *Kikuchi* teaches and motivates [see abstract and Figs. 1, 2, 9 for example] forming an electrode pattern in the surrounding (non-display) region, which when supplied with a voltage acts to trap ionic impurities; this accomplishes the desirable goal of preventing an uneven display.

Likewise, *Tanaka* discloses [see Fig. 1] the same type of electrodes [4] and it would be obvious to one of ordinary skill in the art to incorporate this into the device of *Mitsui* in view of *Kikuchi*, motivated by the improvement in image quality shown by having the dummy electrode pattern of *Tanaka* [compare Figs. 3 and 4 of *Tanaka*].

The electrode of *Tanaka*, taken to be the segments [4] on both substrates, is disposed to surround the pixel display area on all sides, meeting the first additional limitation of claim 15. Alternatively, the electrode pattern can be taken (considering the language of claim 8) to be just the segments, individually addressed, on the lower substrate of *Tanaka*, meeting the first additional limitation of claim 8. The only remaining limitation (in both claims) is that the pattern be coplanar with the pixel electrodes.

Neither *Kikuchi* nor *Tanaka* disclose pixel electrodes; both references teach the use of ion-trapping electrodes using the example of a passive matrix display, with one set of address lines on each substrate, whose intersections are the pixel regions. The other type of display, an active matrix display as disclosed by *Mitsui*, has both sets of address lines forming a grid of pixel regions on one substrate, with transistors (for instance) at each intersection to control a pixel electrode. The question is, where would the ion-trapping electrode patterns be placed in an active matrix device like that of *Mitsui*? The crucial point is that in active matrix displays, the pixel electrodes create electric fields to affect the liquid crystal, while in passive matrix displays, the address lines themselves do this. Therefore, it is the pixel electrodes, not the gate and source lines, which are the analogous structure to the address lines of a passive matrix device.

Thus, one of ordinary skill in the art (such as *Kikuchi* or *Tanaka* who make the electrode pattern coplanar with the address lines) would find it obvious to make the electrode pattern coplanar with the pixel electrodes, when modifying the device of *Mitsui* to have the ion-trapping electrode patterns of *Kikuchi* or *Tanaka*. Claims 8 and 15 are therefore unpatentable.

Allowable Subject Matter

4. Claims 1-7 and 9-14 are allowed.

5. The following is an examiner's statement of reasons for allowance:

Regarding claim 1, the applicant has amended to add the limitation that "the continuous electrode pattern for adsorbing an ionic impurity is provided on only one of the substrates and is at least partially coplanar with the pixel electrodes". Neither *Kikuchi* nor *Tanaka* discloses a continuous electrode pattern surrounding the display pixel area on all sides on only one of the substrate. *Kikuchi* shows the pattern on both substrates along only one edge, while *Tanaka* shows a discontinuous pattern which is on the lower substrate on the right and left sides, while on the upper substrate on the top and bottom sides. Claim 1 is therefore allowable, as are claims 2-7, 11, and 14 which depend on it.

Similarly, the applicant has amended claim 10 to add the limitation that the electrode pattern is "on only one of the substrates, said pattern being coplanar with the pixel electrodes". Since the claim recites the electrode pattern being on only one of the

substrates, and both *Kikuchi* and *Tanaka* disclose having it on both substrates, claim 10 is also allowable.

Claims 9, 12, and 13 recite the electrode pattern for adsorbing an ionic impurity being only along 2 or 3 particular sides of the display, which is not disclosed by the prior art (*Tanaka* discloses the electrode pattern on all four sides, *Kikuchi* discloses it only on one side, that recited by the present claim 10). Claims 9, 12, and 13 are therefore allowed.

Conclusion

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andrew Schechter whose telephone number is (703) 306-5801. The examiner can normally be reached on Monday - Friday, 9:00 - 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, William Sikes can be reached on (703) 308-4842. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-4711 for regular communications and (703) 746-4711 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

AS
Andrew Schechter
October 22, 2002

TOAN TON
PRIMARY EXAMINER